REMARKS

Petition for Extension of Time Under 37 CFR 1.136(a)

It is hereby requested that the term to respond to the Examiner's Action of September 14, 2006 be extended three months, from December 14, 2006 to March 14, 2007.

Authorization to charge a Credit Card is given to cover the extension fee. The Commissioner is hereby authorized to charge any additional fees associated with this communication to Deposit Account No. 19-5425.

In the Office Action, the Examiner indicated that claims 1 through 43 are pending in the application and the Examiner rejected all claims.

The §101 Rejection

On page 2 of the Office Action, the Examiner has rejected claim 1 under 35 U.S.C. §101 as being directed to non-statutory subject matter for failing to utilize any physical element.

Applicant has amended claim 1 to recite that the method steps are performed by a "processor generation tool".

Support for this amendment is found, for instance, in the specification at page 8, which reads, in relevant part:

> "The overall tool chain and relationships between the tools is shown in Figure 6. The box 601 represents the processor generation tool. This takes as input executable code for a host processor 608 and various configuration files 609. Alternatively the tool 601 may provide a graphical user interface allowing direct control of configuration parameters from within the tool. The tool reads and writes descriptions 602 of candidate processor

architectures. In one possible flow through the tool a hardware description of a processor may be generated 612."

Applicant submits that by this amendment, claim 1 is now in compliance with 35 USC §101. Applicant therefore requests that this rejection be withdrawn.

The §112 Rejections

On page 2 of the Office Action, the Examiner has rejected claims 1-43 under 35 U.S.C. §112, second paragraph, as being indefinite. In particular, claim 1 is rejected for failing to recite any procedural steps and failing to make clear what physical processes are performed.

Applicant has amended claim 1 to recite the procedural steps and make clear what physical processes are performed, namely:

(a) a processor generation tool taking, as an input, executable code for an existing and different type of microprocessor (the "second microprocessor");

(b) the processor generation tool reading a description of the architecture of the target microprocessor, as defined by an instruction set;

(c) the processor generation tool automatically adapting the instruction set of the architecture of the target microprocessor at design time, in dependence on the requirements of the executable code of the second microprocessor.

Applicant submits that by this amendment, claim 1 is now in compliance with 35 USC §112, second paragraph. Applicant therefore requests that this rejection be withdrawn.

The Examiner also rejects claim 43 for failing to recite any functional element. Applicant has amended claim 43 to recite a functional element, namely, claim 43 now recites that the microprocessor:

> "stores, and operates using, an instruction set that has been automatically adapted, in dependence on the requirements of executable code of a second existing microprocessor of a type differing from that of said the first microprocessor, by the processor generation tool."

Claim Rejections, 35 U.S.C. §102

On page 3 of the Office Action, the Examiner rejected claims 1 and 43 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,477,683 to Killian et al.

The Cited Prior Art Does Not Anticipate the Claimed Invention

The MPEP and case law provide the following definition of anticipation for the purposes of 35 U.S.C. §102:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP §2131 citing *Verdegaal Bros. v. Union Oil Company of California*, 814 F.2d 628, 631, 2 U.S.P.Q. 2d 1051, 1053 (Fed. Cir. 1987)

The Examiner Has Not Established a *prima facie* Case of Anticipation

The Office Action suggests that Killian discloses the step of using executable code for another type of microprocessor in order to automatically adapt the instruction set of the microprocessor architecture at design time in dependence on the requirements of the executable code (col. 6, lines 53 – 61).

Applicant submits that Killian says "...uses a description of (the) *customized* processor instruction set..." (col. 6, line 53).

In Killian, this customized description is created manually for the target microprocessor to be configured:

> "A user, e.g. a system designer, develops a configured instruction set architecture. That is, using the ISA definition and tools previously developed, a configurable instruction set architecture following certain ISA design goals is developed" (col. 7, lines 10 – 14).

So Killian starts the process of designing a target microprocessor by using an instruction set that has already been customized for that target microprocessor.

The present invention is predicated on the idea of automatically configuring the requirements of the instruction set for the new, target microprocessor by using code previously compiled for a *an existing and different* (and probably 3rd party) microprocessor.

Killian makes no reference in the cited section, or indeed anywhere else, to configuring the ISA of a target microprocessor by reading and adapting the ISA of an existing but different

microprocessor. Killian in fact requires the ISA of the target to start off already customized for that target.

In order to further clarify this distinction and to more clearly distinguish applicant's invention from the prior art, applicant has amended claim 1 to read, with the relevant part italicized:

(a) a processor generation tool taking, as an input, executable code for *an existing* microprocessor *of a second type differing from said first type*;

(b) the processor generation tool reading a description of the target microprocessor architecture, as defined by an instruction set;

(c) the processor generation tool automatically adapting the instruction set of the target microprocessor architecture at design time, in dependence on the requirements of the executable code of the *existing* microprocessor.

In order to further clarify this distinction and to more clearly distinguish applicant's invention from the prior art, applicant has amended claim 43 to read, with relevant part italicized:

A first microprocessor programmed with an architecture that has been automatically configured by a processor generation tool, in which the first microprocessor stores, and operates using, an instruction set that has been automatically adapted, in dependence on the requirements of executable code of a second *existing* microprocessor *of a type differing from that of said the first microprocessor*, by the processor generation tool.

Applicant submits that these amendments place independent claims 1 and 43 in condition for allowance and therefore requests that these claims, as amended, now be allowed.

Applicant submits that claims 2 - 42 each depend from, and include all the limitations of, a now allowable independent claim. Applicant therefore requests that these claims, as amended, now be allowed.

Conclusion

In view of the foregoing amendments and remarks, applicant respectfully requests entry of the amendments, favorable reconsideration of the application, withdrawal of all rejections and objections and that claims 1 - 43 be allowed at an early date and the patent allowed to issue.

Included herein is a Petition for extension of time to respond to the Examiner's Action, and authorization to charge the extension fee to a credit card. The Commissioner is hereby authorized to charge any additional fees or credit any overpayment associated with this communication to Deposit Account No. 19-5425.

Respectfully submitted

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Date

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